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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10015209	11/16/2001	438	1	2825	THOMPSON

**APPLICANTS: Hashimoto Eiki;

**CONTINUING DATA VERIFIED:
NONE

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 354306/2000 11/21/2000 VERIFIED

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☒ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☒ yes ☐ no		NEKU 19.181
Verified and Acknowledged Examiners's initials			

TITLE : Semiconductor circuit designing apparatus and a semiconductor circuit designing method in which the number of steps in a circuit design and a layout design is reduced

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G.
ISSUE FEE: Amount Due / Date Paid			DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER		Primary Examiner / PREPARED FOR ISSUE	Application Examiner

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